

The Cryogenic DC Behavior of Cryo3/AZ1 InP 0.1-by-80-Micrometer-Gate High Electron Mobility Transistor Devices

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We have examined the cryogenic DC behavior of 80-micrometer-gate-width devices from the “Cryo3/AZ1” wafer lot. Our measurements indicate that transistors from all five wafers have good “quality of pinch-off.” The gate-source leakage current and excess gate current have been investigated. All measured devices exhibited memory in the bias behavior at cryogenic temperatures. Illumination of the devices tends to make them more well-behaved. The effect of voltage stress and light on the turn-on voltage of a device from the -041 wafer has been investigated. A weak persistence of the effect of bias stress is also observed.

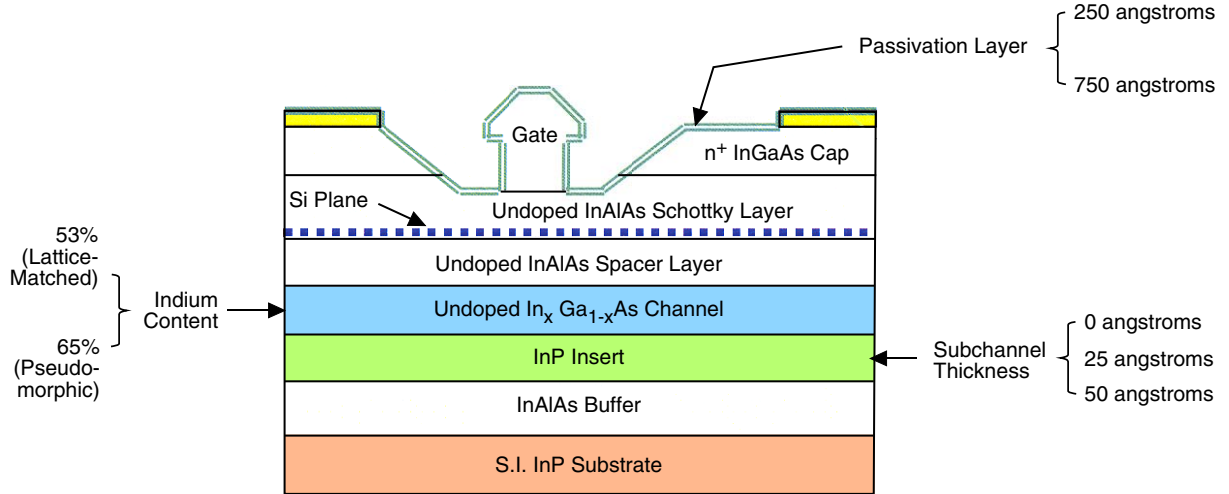
I. Introduction

The “Cryo3/AZ1” wafer run consisted of six wafers fabricated in 1999 by TRW [now Northrop-Grumman Space Technology (NGST)]. The wafers consisted of discrete high electron mobility transistors (HEMTs) having a variety of gate widths (20 to 300 micrometers) for operation between 1 and 100 GHz. The HEMTs utilize a wide bandgap semiconductor (InAlAs) grown on top of a narrow bandgap semiconductor (InGaAs) using molecular beam epitaxy. The quantum well created at the interface is populated with electrons that diffuse from a silicon-doped region in the InAlAs layer. Slightly different epitaxial layers and/or passivation layer thicknesses were used for each wafer. Five of the six wafers survived processing, and their cross-sectional geometry is shown in Fig. 1. Devices from the wafer (TRW designation 4044-041) are used in JPL discrete InP HEMT-based low-noise front-end amplifiers delivered to the Deep Space Network (DSN). They are also used in radio astronomy antennas in the Chilean Atacama desert. Specifically, they are used in National Radio Astronomy Observatory (NRAO) amplifier modules for the Large Millimeter Array and the California Institute of Technology’s Cosmic Background Imager.

This article will present data on sample devices from all five wafers. All the measured devices were four-finger devices with a total gate width of 80 micrometers. The devices used air bridges to provide source connections for all the fingers. The primary aim of this work was to determine the potential low-noise performance of the other wafers and to examine the effect of light and voltage stress on device behavior at 15 K. The low-noise potential was determined by examining the quality of pinch-off of the

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Wafer 4099-040 (Pseudomorphic InGaAs Channel, 750 Å Passivation Layer, 50 Å InP Insert)
 Wafer 4044-041 (Pseudomorphic InGaAs Channel, 250 Å Passivation Layer, 25 Å InP Insert)
 Wafer 4080-055 (Lattice-Matched InGaAs Channel, 750 Å Passivation Layer, 25 Å InP Insert)
 Wafer 4080-057 (Lattice-Matched InGaAs Channel, 750 Å Passivation Layer, 50 Å InP Insert)
 Wafer 4074-090 (Pseudomorphic InGaAs Channel, 750 Å Passivation Layer, No InP Insert)

Wafer 4094-038 (Pseudomorphic InGaAs Channel, 250 Å Passivation Layer, No InP Insert)
 (This Wafer Did Not Survive Processing)

Fig. 1. Cross-sectional view of NGST Cryo3/AZ1 indium phosphide HEMT structure.

transconductance and the gate leakage current. The examination of light and memory bias was stimulated by the observation of hysteresis and tuning difficulties in some low-noise amplifier modules. We wanted to determine if this behavior was intrinsic to the device. This study also was conducted to establish a baseline against which future devices can be compared, since the devices from wafer 4044-041 are among the lowest noise HEMT transistors ever produced. These data can be compared to the “Cryo-11” wafer discrete devices fabricated at NGST in March 2007.

The organization of this article is as follows: Section II presents a brief discussion of the experimental test setup and its validation. Section III presents a comparative assessment of the five wafers in terms of turn-on voltage, quality of pinch-off, gate leakage current, and excess gate current. Section IV presents data showing the memory bias behavior and the effect of illumination. Section V presents a brief discussion of the topics of carrier trapping and impact ionization. These topics are often used to explain some of the behavior seen in Section IV. Some recommendations are presented in Section VI.

II. Experimental Test Setup

The data were taken with a Hewlett-Packard (HP) 4155C semiconductor parameter analyzer and cryogenic wafer probe station [1]. The probe station cooling is provided by a CTI-Cryogenics model 350 Gifford–McMahon closed-cycle helium refrigerator. Coupling between the 15-K cooler cold head and the cold stage on which the devices are mounted is provided by flexible copper braid. The cryocooler first stage cools a radiation shield that encloses the device test area. The probe tips used for this study were coaxial 50-micrometer pitch ground–signal–ground air coplanar probes. They are mounted on the end of a fiberglass rod for thermal isolation and housed inside flexible metal bellows. The fiberglass support rod is attached to the base of the bellows. Movement of the probes in three perpendicular dimensions

plus rotation for planarity is provided by attachment of the base of the bellows to optical stages with micrometer adjustment at room temperature. The DC voltages were placed on the coaxial line using HP 11612B bias networks. This allows placement of 50-ohm terminations on the coaxial lines feeding the transistor. This is an important consideration when testing high-performance transistors that are prone to oscillation in an unmatched environment.

Several tests were conducted to verify proper operation of the parameter analyzer and bias tees. Precision 1.0-megohm and 0.1-ohm resistors were placed on the output cables of the parameter analyzer in order to check the system at high and low current levels. The current leakage of the bias tees was checked by measuring the current-voltage (I-V) behavior with the probe tips raised. This is shown in Fig. 2 for voltages of -0.4 to $+0.4$ volts on port 1 and a fixed 0.9 volts on port 2. For the major portion of the sweep, the leakage current on port 1 was less than a few picoamperes. The leakage current on port 2 for the majority of the sweep was less than 10 picoamperes. This is the worst-case behavior. As expected, smaller voltages give smaller leakage currents. In order to determine the total DC resistance between the parameter analyzer and the probe tips, current-voltage data were taken with the probe tips placed on the shorting bar of a coplanar waveguide calibration substrate. The slopes of the curves indicated the total line resistance from the parameter analyzer to the probe tips to be 1.21 ohms and 1.28 ohms on ports 1 and 2, respectively.

III. Turn-On Voltage, Quality of Pinch-Off, Gate Leakage, and Excess Gate Current

The five wafers do not all have the same turn-on voltage. For the purposes of this article, the turn-on voltage is defined as the gate voltage for which the drain current is 50 microamperes for the specified drain voltage. We have avoided use of the term “threshold voltage” to emphasize that our definition differs from more conventional definitions. The threshold voltage is determined by such factors as the gate-channel spacing, Schottky barrier potential, impurity doping levels, and the difference in the InAlAs/InGaAs

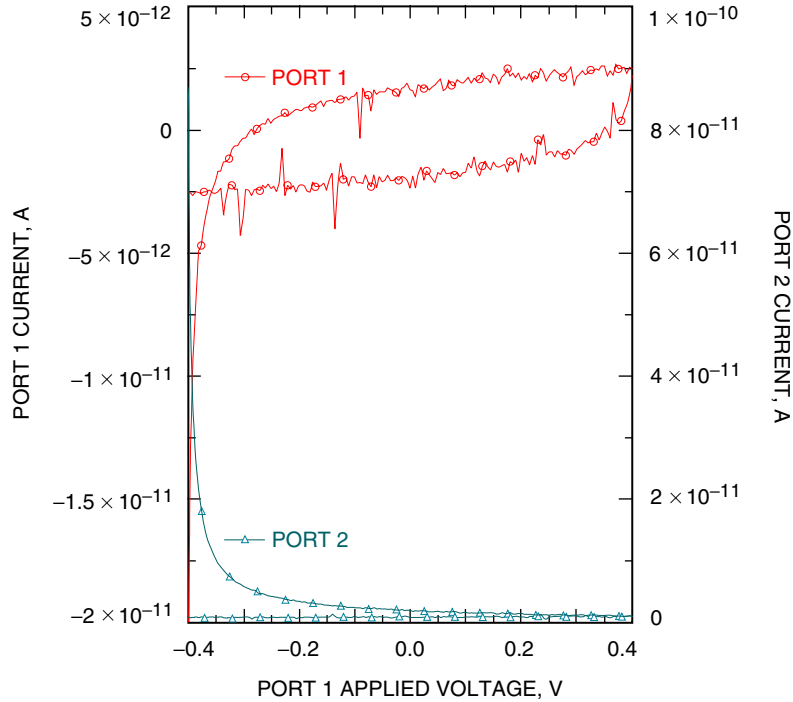


Fig. 2. Double sweep of ports 1 and 2 with the air coplanar probes raised above the device. Port 1 (circle) is used for gate-source measurements, and port 2 (triangle) is used for drain-source measurements. Applied voltage on port 2 was a fixed 0.9 V.

bandgap discontinuity. For short channel devices, such as those studied here, the control of electrons under the gate by the drain is significant. Therefore, when discussing the turn-on voltage, the drain-source potential also must be specified. The measured turn-on voltages at room temperature and 15 K are shown in Table 1. The devices were cooled with no applied bias voltages. The drain-source voltage was 0.9 volts during the measurement.

With the exception of wafer -090, the shift in turn-on voltage upon cooling is within ± 10 percent of the average value of 0.213 volts. The different turn-on voltages of the five wafers at 15 K is clearly seen by plotting the transconductance versus gate voltage for the five wafers. This is shown in Fig. 3. The gradual turn-on behavior of wafer -090 at 15 K is qualitatively different from the other four wafers. The large slope in the linear region of the transconductance versus gate voltage is indicative of the high electron mobility at cryogenic temperatures.

Table 1. Measured turn-on voltages at room temperature and 15 K ($V_{ds} = 0.9$ V).

Wafer	Turn-on voltage (296 K), V	Turn-on voltage (15 K), V	Shift
-090	-0.282	-0.206	+0.076
-055	-0.196	+0.016	+0.212
-041	-0.186	+0.005	+0.191
-040	-0.185	+0.029	+0.214
-057	-0.042	+0.192	+0.234

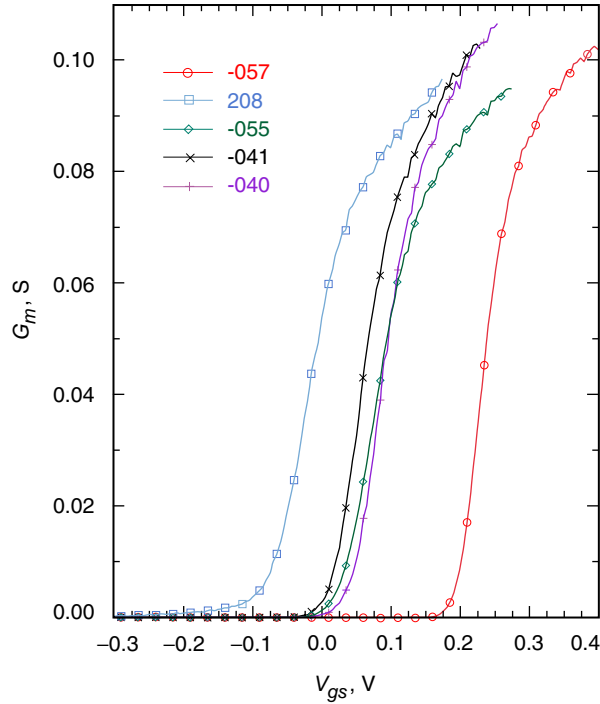


Fig. 3. Transconductance versus gate voltage (single sweep) for a sample device from all 5 wafers at 15-K physical temperature. The drain voltage was 0.9 V: wafers -057 (circle), -090 (square), -055 (diamond), -041 (X), and -040 (+).

Two features that are indicators of the potential low-noise performance of a device are the “quality of pinch-off” of the transconductance and the gate leakage current. The reader is referred to the excellent articles by Pospieszalski [2,3] for a more in-depth discussion of these topics and a two-parameter noise model he developed. (In the most general case, four noise parameters are needed at each frequency to completely characterize a noisy two-port.) In the Pospieszalski noise model, the bias, frequency, and temperature dependence of the transistor noise parameters can be approximately predicted if an equivalent gate and drain temperature are known. His model has proved useful because experience has shown that in III-V semiconductor devices, the equivalent gate temperature is largely independent of bias and approximately equal to the physical temperature of the device. In addition, the equivalent drain temperature is largely independent of temperature but strongly dependent on the bias. In many cases, the drain temperature dependence on drain current is roughly linear.

According to the Pospieszalski model [3], the minimum noise temperature of the device is given by

$$T_{\min} = 2 \frac{f}{f_t} \sqrt{g_{ds} T_d r_{gs} T_g + \left(\frac{f}{f_t} \right)^2 r_{gs}^2 g_{ds}^2 T_d^2} + 2 \left(\frac{f}{f_t} \right)^2 r_{gs} g_{ds} T_d \quad (1)$$

The second term under the radical sign as well as the second term on the right-hand side can be omitted in the limit where

$$\left(\frac{f}{f_t} \right)^2 \ll \frac{T_g}{T_d} \frac{1}{r_{gs} g_{ds}} \quad (2)$$

In this limit, the minimum noise temperature is given approximately by

$$T_{\min} \cong 2 \frac{f}{f_t} \sqrt{g_{ds} r_{gs} T_g T_d} \quad (3)$$

In these equations, f is the frequency of operation, f_t is the transistor cut-off frequency, g_{ds} is the drain-source conductance, T_d is the equivalent drain temperature, r_{gs} is the gate-source resistance, and T_g is the equivalent gate temperature. Also, $f_t = g_m / 2\pi C_{gs}$, where g_m is the transconductance and C_{gs} is the gate-source capacitance. Reference [2] or [3] provides the intrinsic field-effect transistor (FET) equivalent circuit diagram to which the above equations apply. As mentioned above, T_g is approximately the same as the device physical temperature. If we assume g_{ds} , r_{gs} , and C_{gs} are approximately bias independent [1] and the drain noise temperature is roughly linear with drain current, then the minimum noise temperature should vary with bias as

$$T_{\min} \sim \frac{\sqrt{I_{ds}}}{g_m} \quad (4)$$

Therefore, a low-noise temperature device is one for which a large value of the transconductance is achieved at a small value of drain current. A device for which this is true is said to have good quality of pinch-off. Figure 4 shows the transconductance versus drain current for device A from wafer -055 at 296 K and at 15 K. The lower T_{\min} potential at 15 K is clearly evident. Figure 5 shows a comparison of transconductance versus drain current for samples from all five wafers at 15 K. In particular, for the samples measured, wafers -040 and -057 have slightly better quality of pinch-off than wafer -041.

In order to obtain high cut-off frequencies, HEMTs have evolved to have short gates deposited on a thin, highly doped layer. This tends to increase the gate leakage current of the Schottky barrier. The

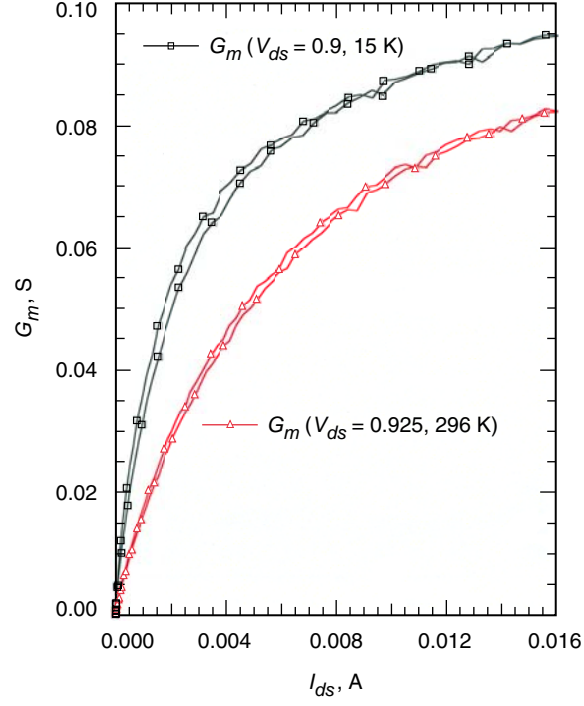


Fig. 4. Transconductance versus drain current (double sweep) for device A from wafer -055 at 15-K (square) and 296-K (triangle) physical temperature. The drain voltage at 296 K was 0.925 V, and at 15 K it was 0.90 V.

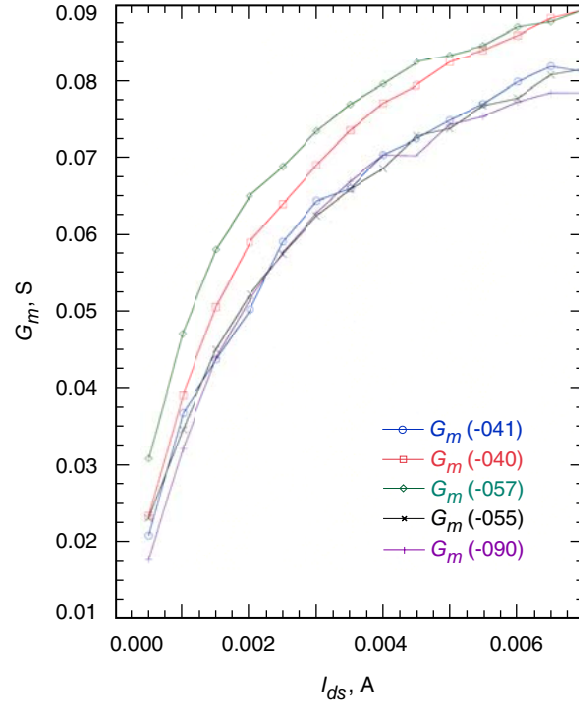


Fig. 5. Transconductance versus drain current (single sweep) for a sample device from all 5 wafers at 15 K. The applied drain voltage was 0.9 V, with no illumination: wafers -041 (circle), -040 (square), -057 (diamond), -055 (X), and -090 (+).

effect of gate leakage current on the noise performance has been studied, and several models have been proposed. In one model, a parallel resistance is added between the gate and source with an associated temperature to account for the leakage current [4]. Most models incorporate the effect of gate leakage current by adding a frequency-independent shot-noise current source at the device input [3,5,6]. The shot-noise current source is in parallel but uncorrelated with the usual thermal noise source associated with the gate temperature T_g .

It is remarked in [2] that the noise source should instead be connected between the gate and drain. However, this situation can be modeled as two perfectly correlated noise currents flowing between the drain and source and the gate and source. The former current source will be much less than that due to the noise contribution associated with the drain temperature T_d and can be neglected. Therefore, both the gate-source and gate-drain leakage currents can be modeled as a shot-noise generator between the gate and source. In this case, the best approximation for the leakage current may be the sum of the absolute values of leakage current between gate-source and gate-drain terminals.² It is noted in [5] that, if the shot noise is due to tunneling of electrons, then the value of I_{gs} to be used in Eq. (6) below is the measured DC gate current. If avalanching effects are occurring, the effective gate current can be much higher.

Following the model presented in [3], the effect of gate leakage on the minimum noise temperature is given by

$$T_{\min}^{\text{Leakage}} = T_{\min} + 2NT_o \left\{ \sqrt{1 + A \left(\frac{f_t}{f} \left| \frac{Z_{\text{opt}}}{R_{\text{opt}}} \right| \right)^2} - 1 \right\} \quad (5)$$

where

$$A = \frac{\overline{i_{gs}^2}}{\overline{i_{ds}^2}} = \frac{qI_{gs}}{2kT_d g_{ds}} \quad (6)$$

Also, $N = R_{\text{opt}}g_n$ and $T_o = 290$ K. The noise conductance is given by

$$g_n = \left(\frac{f}{f_t} \right)^2 \frac{g_{ds}T_d}{T_o} \quad (7)$$

The quantity $Z_{\text{opt}} = R_{\text{opt}} + jX_{\text{opt}}$ is the optimum source impedance. The constant k is Boltzmann's constant, and q is the charge of the electron. The minimum noise temperature without gate leakage current, T_{\min} , is given by Eq. (1). The optimum source resistance and reactance are given by

$$R_{\text{opt}} = \sqrt{\left(\frac{f_t}{f} \right)^2 \frac{r_{gs}T_g}{g_{ds}T_d} + r_{gs}^2} \quad (8)$$

$$X_{\text{opt}} = \frac{1}{\omega C_{gs}}$$

We can show the effect of gate leakage current by inserting suitable values for the variables in Eq. (5) that represent a good InP HEMT device. For example, for a Cryo-3, 200-micrometer-gate-width device

² M. Pospieszalski, personal communication, National Radio Astronomy Observatory, Charlottesville, Virginia, 2007.

from wafer -041 at 15 K, we estimate $r_{gs} = 0.116$ ohms, $g_{ds} = 0.0127$ mhos, $g_m = 0.164$ siemens, $C_{gs} = 0.161$ pF, $T_g = 13$ K, and $T_d = 500$ K. Note that these values are for the intrinsic chip and do not include the effects of gate, source, and drain-pad resistance and inductance. Table 2 shows the effect of various gate leakage currents on T_{\min} at 8.5 GHz. At 8.5 GHz, a gate leakage current as small as 0.16 microamperes will cause the device to have roughly three times the intrinsic minimum noise temperature of a device with no gate leakage current. Table 3 shows the same calculation at 32 GHz. In this case, a gate leakage current of about 2.5 microamperes will cause the device to have roughly three times the intrinsic minimum noise temperature of the device with no gate leakage current.

Figure 6 shows a comparison of the gate leakage current at 15 K for sample devices from the five wafers at zero drain volts. These data suggest that the other four wafers have leakage comparable to wafer -041, a wafer with proven low-noise devices. However, data taken at zero drain volts may not be a reliable indicator of gate leakage under low-noise bias conditions. Other interesting effects can occur for larger values of drain voltage. Figure 7 shows the gate current versus gate voltage for a device from wafer -041 at drain voltages of 0.1, 0.5, and 0.9 volts. The gate-source current at 0.1 and 0.5 volts is probably due to electron tunneling. The gate current at 0.9 volts shows a large peak at $V_{gs} = 0.16$ volts. This behavior is normally attributed to impact ionization. Impact ionization is an inelastic collision process involving an electron that has gained energy from the electric field. At high drain-source voltages, impact ionization

Table 2. Effect of gate leakage currents on T_{\min} at 8.5 GHz.

$I_{gs}, \mu\text{A}$	T_{\min}, K
0.0	0.328
0.04	0.574
0.08	0.742
0.12	0.878
0.16	0.996
0.20	1.101
0.30	1.328
0.40	1.521
0.50	1.692

Table 3. Effect of gate leakage currents on T_{\min} at 32 GHz.

$I_{gs}, \mu\text{A}$	T_{\min}, K
0.0	1.278
0.5	2.115
1.0	2.700
1.5	3.176
2.0	3.589
2.5	3.958
3.0	4.296
3.5	4.608
4.0	4.900

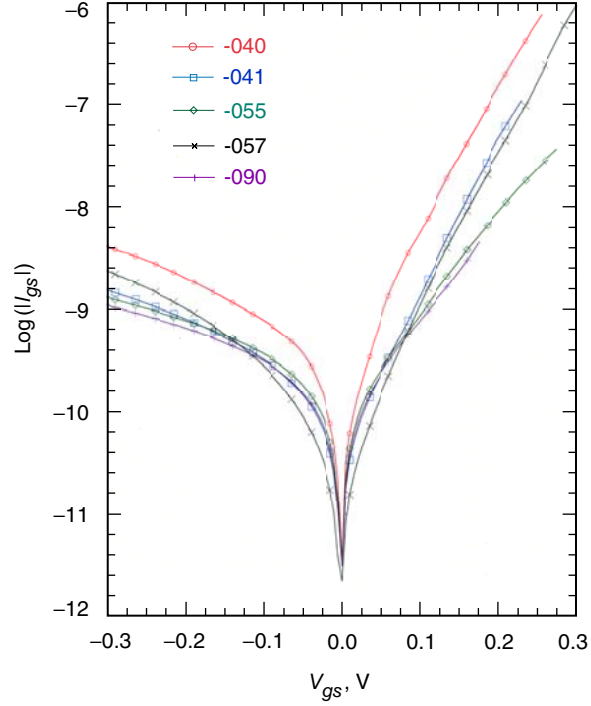


Fig. 6. Logarithm of the absolute value of gate current versus gate voltage (single sweep) at 0 applied drain volts and 15-K physical temperature for a sample device from all 5 wafers: wafers -040 (circle), -041 (square), -055 (diamond), -057 (X), and -090 (+).

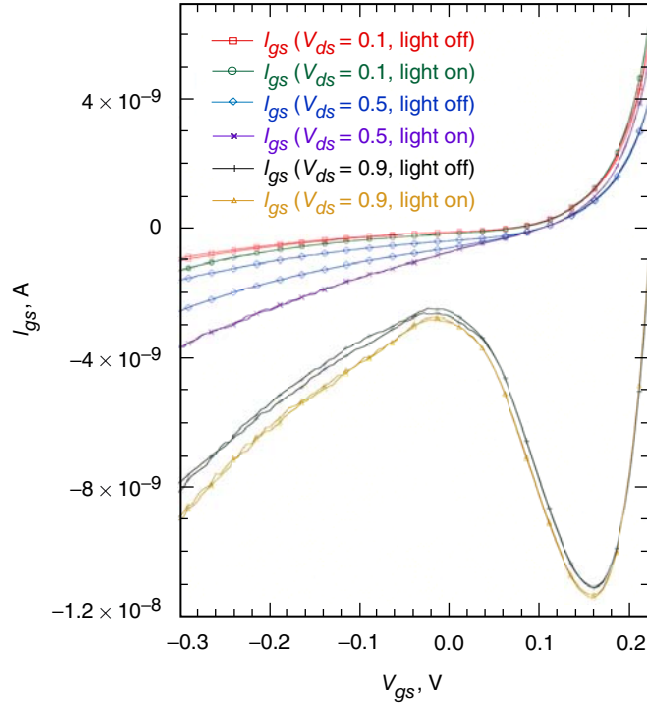


Fig. 7. Gate current versus gate voltage (double sweep) for device E, wafer -041, at 15-K physical temperature, with and without illumination. Applied drain voltages were 0.1 V, light off (square); 0.1 V, light on (circle); 0.5 V, light off (diamond); 0.5 V, light on (X); 0.9 V, light off (+); and 0.9 V, light on (triangle).

can generate additional electron-hole pairs in the channel of the HEMT. These additional carriers cause the gate and drain current to increase. Although the impact ionization in this case raises the gate current, the increase is quite small. The modeling of this impact-ionization-generated gate current on noise performance has been addressed in [7].

Figure 8 shows the gate leakage current at $V_{ds} = 0.9$ volts for all five wafers. From experience, we might argue that the low-noise gate bias would occur when the transconductance is about 50 mS. For wafers -041, -040, and -055, this implies a gate voltage between 50 and 100 mV. In this range, I_{gs} is less than a few hundredths of a microampere. Similarly, devices from wafer -090 would require a gate voltage near zero volts. From Fig. 8, the reverse gate leakage current is again very small, about one hundredth of a microampere. Finally, the device from wafer -057 may require a gate bias voltage of approximately 240 mV. Although under this bias the gate would be drawing a forward current, its magnitude would still be of the order of 0.1 microampere and could yield low-noise performance. The devices from wafers -041 and -090 show clear evidence of an impact ionization component, but the effect is not large.

Another instance when the gate current varies with drain voltage is shown in Fig. 9. This figure shows the gate current versus drain voltage for fixed gate voltages between 55 mV and 230 mV for a device from the -041 wafer at 15 K. The normal low-noise gate-source bias voltage for this device is between 50 mV and 100 mV. The normal low-noise drain bias voltage is approximately 0.9 volts. For these voltages, I_{gs} is small and negative. However, for larger values of gate voltage, the gate current is positive for all values of the drain voltage. More surprisingly, the gate current initially decreases with increasing drain voltage, reaching a minimum around $V_{ds} = 0.45$ volts. Then the current increases again and peaks at about $V_{ds} = 0.8$ volts before falling again. Behavior similar to this is discussed in [8]. Palmateer et al. attribute the increase in gate current to hot (energetic) drain current electrons overcoming the InGaAs/InAlAs barrier and moving into the AlInAs layer. Some of these electrons are collected by the forward-biased gate and some are collected by the drain. A similar effect may be occurring here. The top-most curve

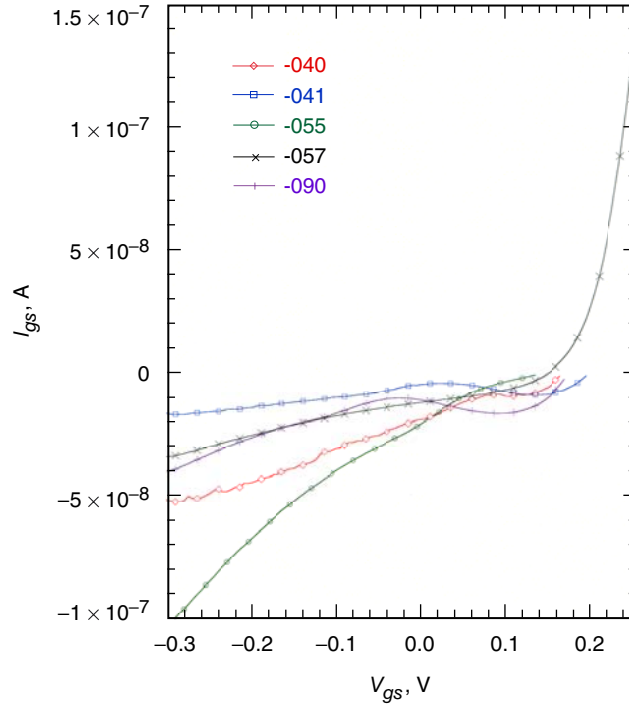


Fig. 8. Reverse gate current versus gate voltage (single sweep) at 15-K physical temperature and 0.9 drain volts. A sample device from each wafer is presented: wafers -040 (diamond), -041 (square), -055 (circle), -057 (X), and -090 (+).

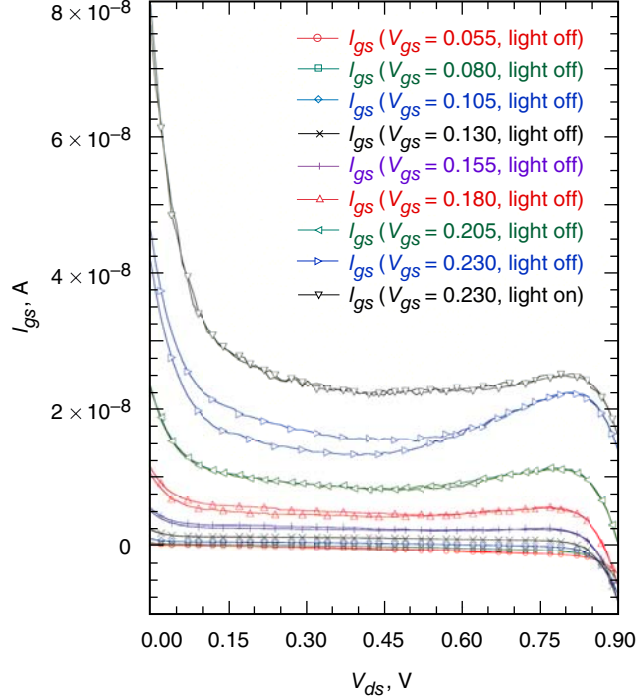


Fig. 9. Gate current versus drain voltage (double sweeps) for stepped values of gate voltage. Data for device C, wafer -041, at 15 K: $V_{gs} = 0.055$, light off (circle); $V_{gs} = 0.080$, light off (square); $V_{gs} = 0.105$, light off (diamond); $V_{gs} = 0.130$, light off (X); $V_{gs} = 0.155$, light off (+); $V_{gs} = 0.180$, light off (up-pointing triangle); $V_{gs} = 0.205$, light off (left-pointing triangle); $V_{gs} = 0.230$, light off (right-pointing triangle); and $V_{gs} = 0.230$, light on (down-pointing triangle).

in Fig. 9 shows the same bias condition with the microscope light turned on. The effect of the light is to slightly raise the gate current, but it also substantially reduces the increase in gate current between 0.5 and 0.8 drain volts.

Figure 10 shows a comparison of this “excess” gate current behavior for the five wafers. A large (but comparable for each device) gate voltage was chosen to enhance the effect. The difference in behavior is marked. Wafers -040 and -041 are seen to be similar in shape, with the device from the -040 wafer having roughly five times the current (right-hand ordinate of the figure). The device from wafer -090, the most “depletion-mode-like,” also has positive gate current for all values of drain voltage. However, the gate current magnitude is the smallest of all the wafers. The shape of the gate current versus drain voltage curve of the -090 device is somewhat similar to those of the -041 and -040 devices. The device from wafer -057, the most “enhancement-mode-like” of all five wafers, has current values roughly 20 times larger than the other wafers. This is perhaps not surprising given the large forward bias on the gate. However, it does not exhibit the large relative increase in gate current, at least over the drain voltage range measured. The most surprising result may be for the device from the -055 wafer. Although its transconductance versus gate voltage is similar to that of wafers -040 and -041, the behavior of the gate current is quite different. Its gate current at zero drain volts is much smaller, and the region of increasing gate current extends from about 0.275 volts to something beyond 0.9 volts, with no sign of turning around. Is this device suffering more from “hot electron” effects than the other wafers? Further investigation is necessary.

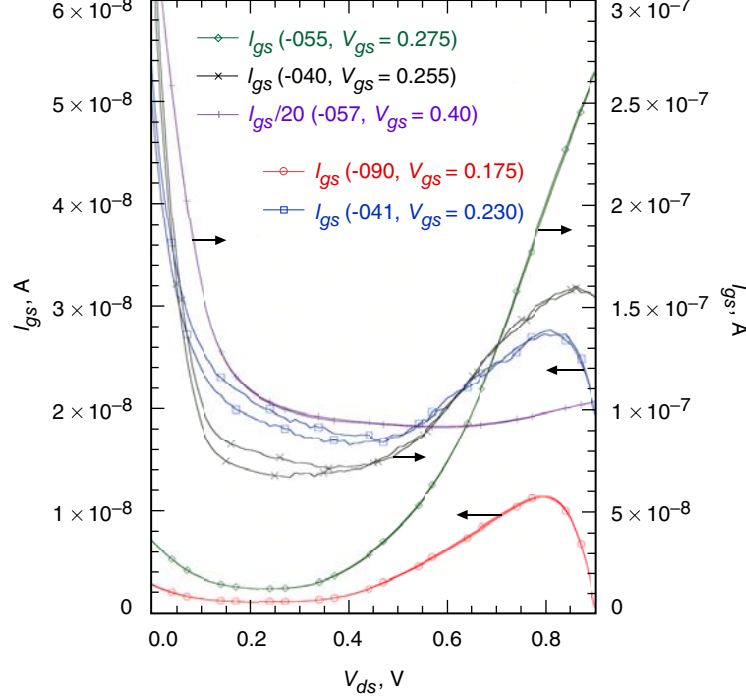


Fig. 10. Gate current versus drain voltage (double sweeps) for a sample device from each wafer at 15-K physical temperature: wafers -055, $V_{gs} = 0.275$ (diamond); -040, $V_{gs} = 0.255$ (X); -057, plotted values are measured values divided by 20, $V_{gs} = 0.40$ (+); -090, $V_{gs} = 0.175$ (circle); and -041, $V_{gs} = 0.230$ (square).

IV. Bias Memory and the Effect of Light

The earliest HEMTs, AlGaAs/GaAs ones in particular, were notoriously sensitive to light and voltage stress at cryogenic temperatures. It is generally accepted that InP HEMTs at cryogenic temperatures are much less sensitive to illumination and voltage stress. Indeed, [9] reported I-V characteristics that were light-independent and did not exhibit hysteresis on similar InP HEMT devices. These devices used 80 percent indium composition in the channel layer and were unpassivated. In contrast, the Cryo-3 devices use either 53 or 65 percent indium composition in the channel and have passivation layer thicknesses of either 250 or 750 angstroms. We have observed interesting signs of memory bias and the effect of illumination. It is possible that the tuning difficulties observed in a significant number of low-noise amplifier modules can be attributed to bias memory of the devices themselves.

The simplest example of bias memory is provided by merely repeating the same I-V measurement in quick succession. Figure 11 shows three sets of drain I-V curves measured in quick succession on a device from wafer -041. For all three sweeps, the gate voltage was increased from 0.105 volts to 0.195 volts in 30-mV steps. All the sweeps were double sweeps. That is, the drain voltage was swept from 0.0 to 0.4 volts and back to 0.0. The collapse of the hysteresis loop, as well as a general turning off of the device with additional sweeps, is clearly evident in the figure. Figure 12 shows the effects of both a fixed, but temporary, voltage stress and light on the drain curves of another device from wafer -041. The first sweep was conducted in the dark before any stress was applied. The second sweep was after the simultaneous application of a drain voltage stress of 0.475 volts and a gate stress of 0.220 volts for 60 seconds. The third sweep is after illumination with the microscope ring light. Again, some collapse of the hysteresis is observed after the temporary bias stress. The application of light clearly raises the drain current, especially for drain voltages below 0.8 volts.

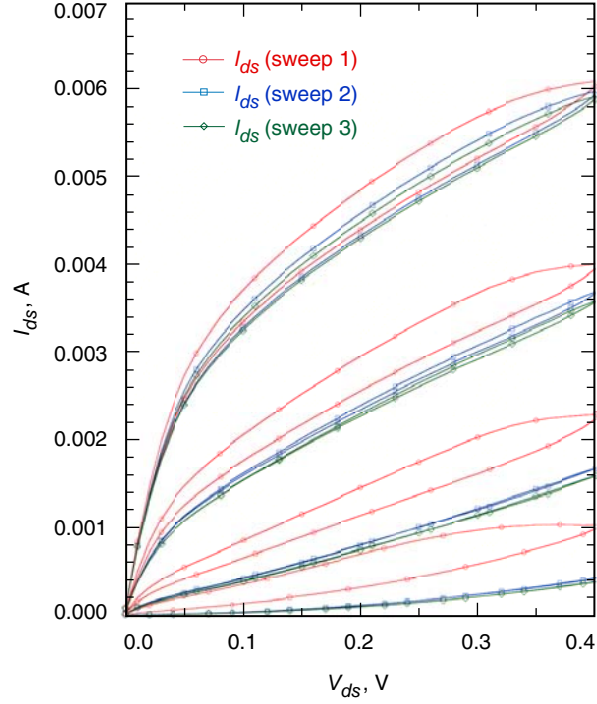


Fig. 11. Three sets of drain current versus drain voltage for device D, wafer -041, at 15 K, taken in quick succession. The gate voltage was 0.105 to 0.195 V in 0.030-V steps: sweeps 1 (circle), 2 (square), and 3 (diamond).

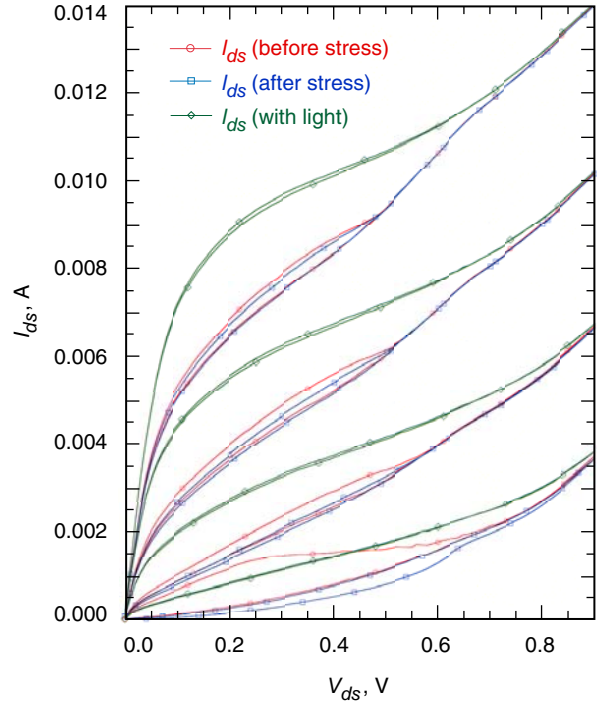


Fig. 12. Effect of voltage stress and light on device E, wafer -041, at 15 K. Three sets of data were taken: sweep 1 (circle), sweep 2 (square) after voltage stress of 0.475 drain volts and 0.220 gate volts for 60 s, and sweep 3 (diamond) with illumination. The gate voltages were 0.100 to 0.220 V in steps of 0.040 V. All sweeps are double sweeps.

Figure 13 shows the effect of illumination on the drain I-V curves for a sample device from wafer -041. Figures A-1 through A-4 in the Appendix show similar behavior is exhibited by samples from the other wafers. The effect of light is to increase the drain current and essentially eliminate the hysteresis. The sudden increase in drain current that typically occurs around $V_{ds} = 0.5$ to 0.6 volts may be indicative of impact ionization occurring in the channel.

Perhaps the most striking effects of both memory and light are shown in Figs. 14 and 15. The plots are conventional sweeps of drain current versus drain voltage for constant, but stepped, increases in gate voltage. Each time the sweep is repeated, the maximum drain voltage is increased. All sweeps are double sweeps. The memory effect is clearly visible in Fig. 14. Figure 15 is the same measurement with the microscope light turned on. In all cases, the curves collapse down to a single set of curves independent of maximum drain voltage. As in Fig. 13, the drain current in the presence of light is larger than the dark drain current. Figures A-5 through A-10 show similar behavior is exhibited by devices from wafers -090, -040, and -057.

Figure 16 shows a similar plot of drain I-V curves with increasing maximum drain voltage for a device from wafer -090. In this case, however, the gate voltage was held fixed. Figure A-11 shows similar behavior for a device from wafer -055. All the data were taken at 15 K.

In an attempt to gain a further understanding of the origin of the bias memory, we investigated its effect on the turn-on voltage. (The turn-on voltage should be sensitive to the presence of deep level traps in the InAlAs.) We examined a device from wafer -041 at 15 K in detail. Figure 17 shows the measured shifts in turn-on voltage in the V_{gs} - V_{ds} plane. The voltage stresses were applied for 60 seconds in the dark. For the range covered, the largest shifts were observed when a combination of gate and drain voltages was applied. When a gate voltage of 0.180 volts and a drain voltage of 0.475 volts were simultaneously applied, a shift of 41 mV was observed. A gate voltage stress alone of 0.230 volts results in only a 0.25-mV

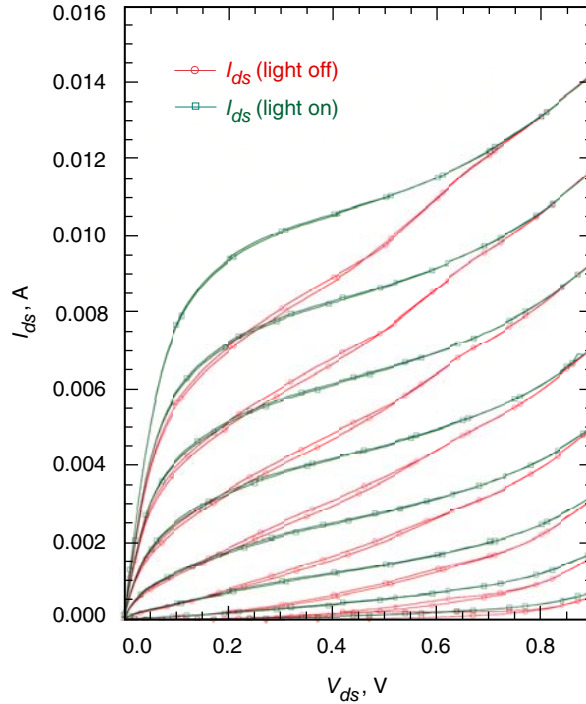


Fig. 13. Drain current versus drain voltage (double sweep) without light (circle) followed by with light (square) for device C, wafer -041, at 15 K. The gate voltage was from 0.055 to 0.230 V in steps of 0.025 V.

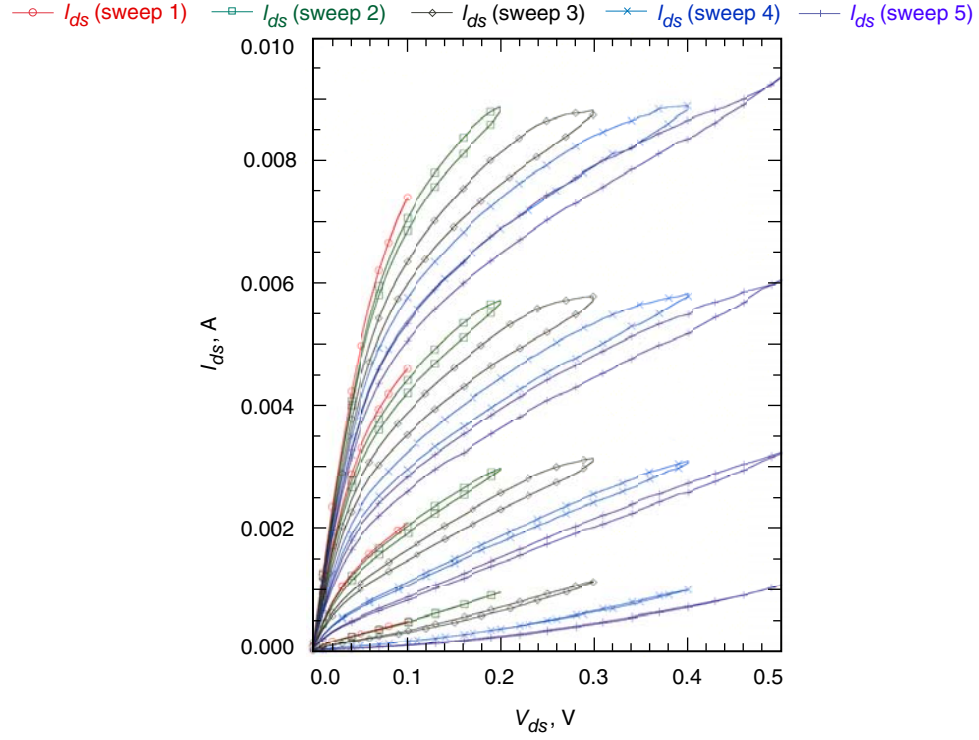


Fig. 14. Drain current versus drain voltage (double sweeps) for device E, wafer -041, at 15 K, with no light. In each data sweep, the gate voltage ranged from 0.100 to 0.220 V in steps of 0.040 V. Maximum drain voltages were 0.1 V (circle), 0.2 V (square), 0.3 V (diamond), 0.4 V (X), and 0.5 V (+).

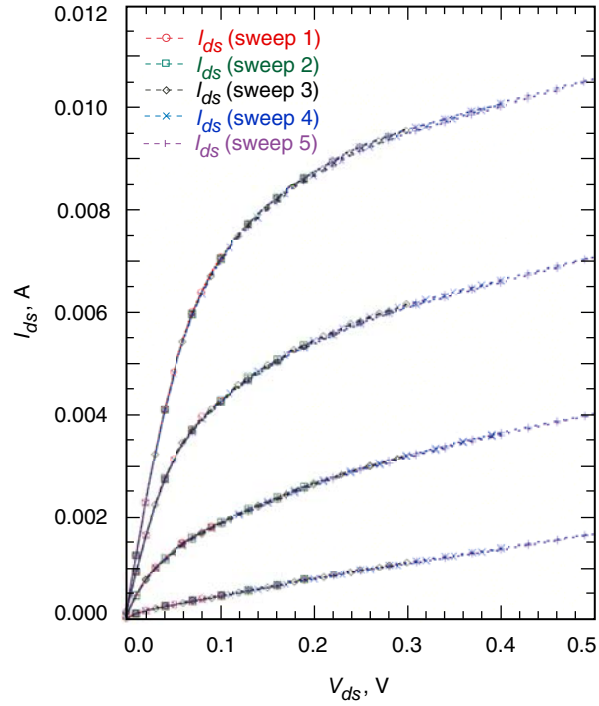


Fig. 15. The same conditions as shown in Fig. 14, but with illumination.

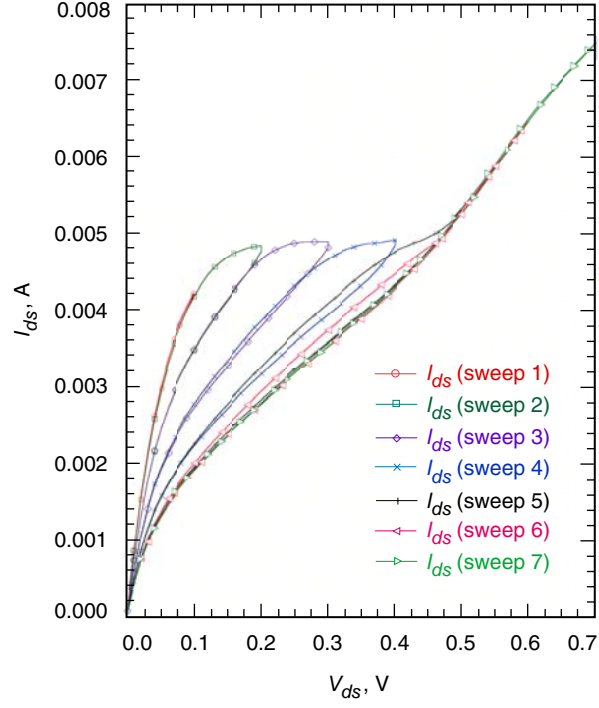


Fig. 16. Drain current versus drain voltage (double sweeps) for device A, wafer -090, at 15 K, with no light. Seven curves are shown. For each curve, the gate voltage was 0.10 V. Maximum drain voltage was 0.1 V (circle), 0.2 V (square), 0.3 V (diamond), 0.4 V (X), 0.5 V (+), 0.6 V (left-pointing triangle), and 0.7 V (right-pointing triangle).

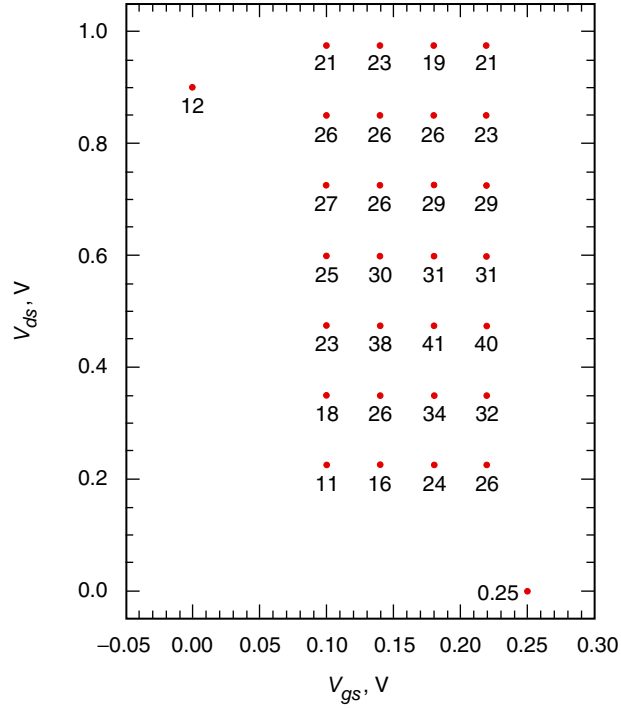


Fig. 17. The shift in turn-on voltage following application of a 60-s bias stress for a variety of voltages in the $V_{ds}-V_{gs}$ plane. The data were taken on device E, wafer -041, at 15 K, with no light. In all cases, the voltage shift was positive.

shift. A drain voltage stress alone of 0.9 volts results in a shift of 12 mV. The subsequent illumination of the device largely returns the transistor to its pre-stressed condition. This was the technique used to “reset” the device prior to application of the next voltage stress. For all determinations of the turn-on voltage, the drain voltage did not exceed 0.1 volts. This was to ensure that the act of determining the turn-on voltage did not affect the measurement of the turn-on voltage.

One may ask whether the change in turn-on voltage is momentary or of longer duration. We did not attempt a careful, systematic study of the time dependence. However, a few measurements were made to ascertain how quickly the voltage stress effect seemed to disappear. Figure 18 shows the behavior for a device from the -057 wafer. The applied voltage stress was $V_{ds} = 1.0$ volts and $V_{gs} = 0.0$ volts for 60 seconds. I-V curves were recorded immediately after application of the stress, and then 5, 10, and 20 minutes later. Even after 20 minutes the pre-stressed condition had not been reached. In some cases, the turn-on voltage actually increased with time after the stress was applied.

We investigated the sensitivity of the turn-on voltage to illumination. We examined the shift in turn-on voltage for two values of the drain voltage. The results are shown in Table 4. In some cases, the data had considerable hysteresis. In these cases, we measured the voltage shifts between the midpoints of the hysteresis loops at 50 microamperes of drain current. These cases are indicated by an asterisk in the table. It can be seen by comparison to Fig. 17 that the shift in turn-on voltage due to light is considerably smaller than can be achieved by some applied voltage stresses.

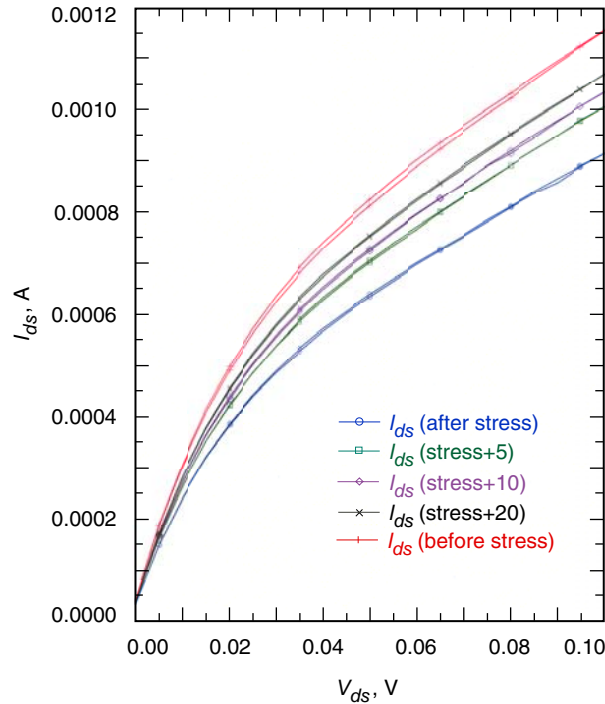


Fig. 18. Drain current versus drain voltage for device B, wafer -057, at 15 K, with no light. The gate voltage during the measurements was 0.275 V. Data are shown prior to the voltage stress (+), immediately after (circle), and 5 minutes (square), 10 minutes (diamond), and 20 minutes (X) after the stress. The voltage stress was 1.0 V on the drain and 0.0 V on the gate.

Table 4. The shift in turn-on voltage due to light.

Wafer	$V_{ds} = 0.1$ V, shift in turn-on voltage, mV	$V_{ds} = 0.9$ V, shift in turn-on voltage, mV
-090	-4*	+1
-040	+5*	-9
-041	+2*	-2*
-055	-5	-1*
-057	-4	-6*

*Shift evaluated between midpoints of hysteresis loops.

V. Discussion

Some of the behavior seen in the previous sections is probably attributable to trapping and de-trapping of carriers from deep levels, impact ionization, or a combination of both. Since these topics are often invoked in the literature as explanations, a brief discussion of these topics will now be presented. Doping naturally creates “imperfections” in the lattice structure which can lead to trapping of electrons. An elementary discussion of the physics involved in trapping by imperfections for a simple one-dimensional string of atoms can be found in [10]. In the electron device literature, donor-related traps usually are referred to as donor complex (DX) centers. These have been observed in many III-V semiconductors. To the author’s knowledge, the microscopic structure of these levels is still controversial, although they are believed to be states of the isolated substitutional donor. DX centers were widely used to explain the I-V collapse seen in the early AlGaAs/GaAs HEMTs. An excellent review of DX centers in III-V compounds can be found in [11].

The nature of the DX centers in InP HEMTs is less clear. One group that examined the possibility of DX centers in $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ grown on Sn-doped InP substrates [12] found evidence of deep electron trapping centers that correlated with the silicon-doping concentration. They also observed a weak persistent photoconductivity effect. In terms of the impact on noise temperature, at least one group notes that additional generation-recombination noise due to the presence of traps must be considered at lower frequencies [4].

In general, the impact ionization rate is dependent on lattice temperature, orientation, strength of the electric field, and alloy composition [13]. It has been invoked to explain the “kink effect.” This is a sudden increase in the drain current at certain drain-to-source voltages. This leads to high drain conductance (g_o), transconductance (g_m) compression, and poor linearity. Since the voltage gain of the device depends on g_m/g_o , this leads to low voltage gain.

The effect of impact ionization on the noise temperature has also been modeled [7]. This model represents the additional electron-hole pair generation due to impact ionization by a voltage-controlled current noise source in the transistor output circuit. The controlling voltage is the intrinsic gate-drain voltage. Since the carrier generation due to impact ionization depends on a spatially varying electric field, no simple analytical expression is known for the relation between bias conditions and the noise current. Like the gate leakage current, this impact ionization noise current leads to a higher minimum noise temperature. It also affects the value of Z_{opt} and the noise resistance.

VI. Recommendations

It is recommended that experiments be conducted using red light-emitting diodes (LEDs) to illuminate the devices in low-noise amplifier (LNA) modules that exhibit tuning difficulties. X-band (8.5-GHz) low-noise amplifier modules using devices from each of the five wafers have been built and tested. They have all yielded good low-noise performance. It would be useful to correlate this good low-noise performance with on-wafer DC and radio frequency (RF) measurements. Therefore, it is recommended that larger-gate-width devices be studied, since these are the devices used at lower frequencies. A comparison of the low-noise performance and tuning behavior of unpassivated devices with 80 percent indium concentration in the active channel should also be made. As these reportedly did not exhibit light or hysteresis effects, further understanding of these effects on amplifier performance may be gained.

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Appendix

Additional Cryogenic DC Data

Figures A-1 through A-4 are similar to Fig. 13, but apply to devices from wafers -090, -055, -040, and -057, respectively. Figures A-5 through A-10 are similar to Figs. 14 and 15, but apply to devices from wafers -090, -040, and -057, respectively. Figure A-11 is similar to Fig. 16, but applies to a device from wafer -055.

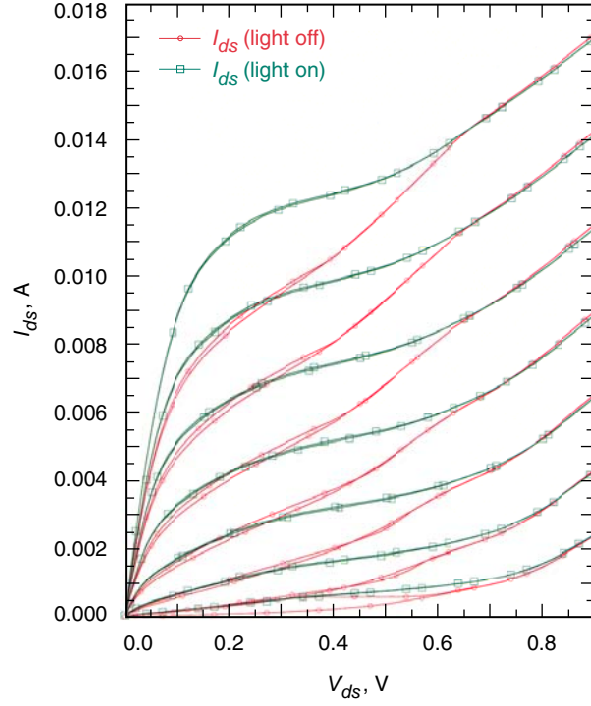


Fig. A-1. Drain current versus drain voltage (double sweep) for device A, wafer -090, at 15 K. Data were taken with the light off (circle), followed by the light on (square). The gate voltage was from 0.0 to 0.180 V in steps of 0.030 V.

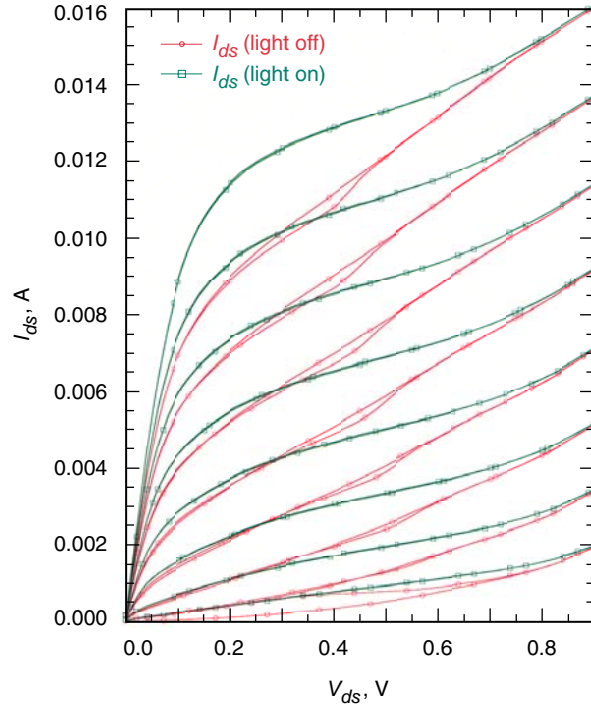


Fig. A-2. Drain current versus drain voltage (double sweep) for device C, wafer -055, at 15 K. Data were taken with the light off (circle), followed by the light on (square). The gate voltage was from 0.10 to 0.275 V in steps of 0.025 V.

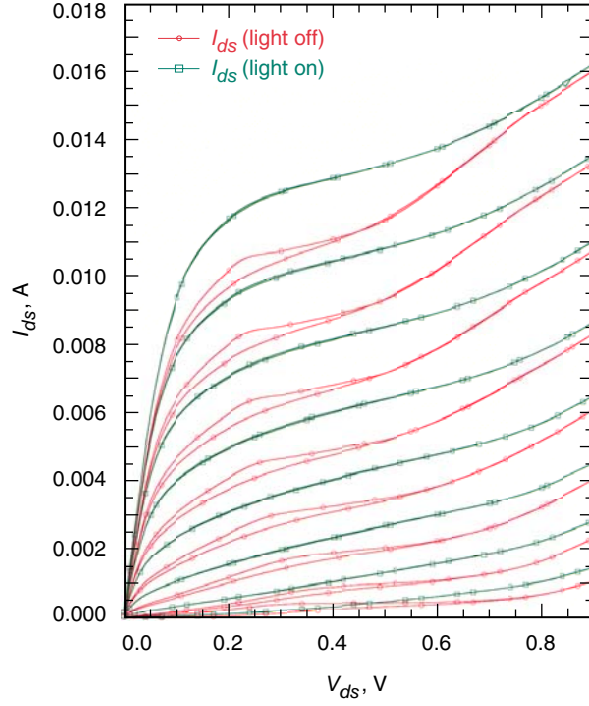


Fig. A-3. Drain current versus drain voltage (double sweep) for device B, wafer -040, at 15 K. Data were taken with the light off (circle), followed by the light on (square). The gate voltage was from 0.080 to 0.255 V in steps of 0.025 V.

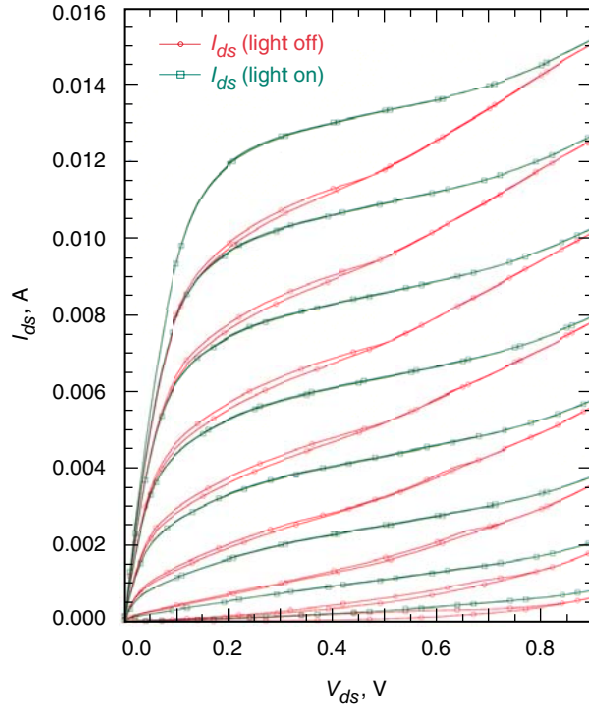


Fig. A-4. Drain current versus drain voltage (double sweep) for device B, wafer -057, at 15 K. Data were taken with the light off (circle), followed by the light on (square). The gate voltage was from 0.225 to 0.400 V in steps of 0.025 V.

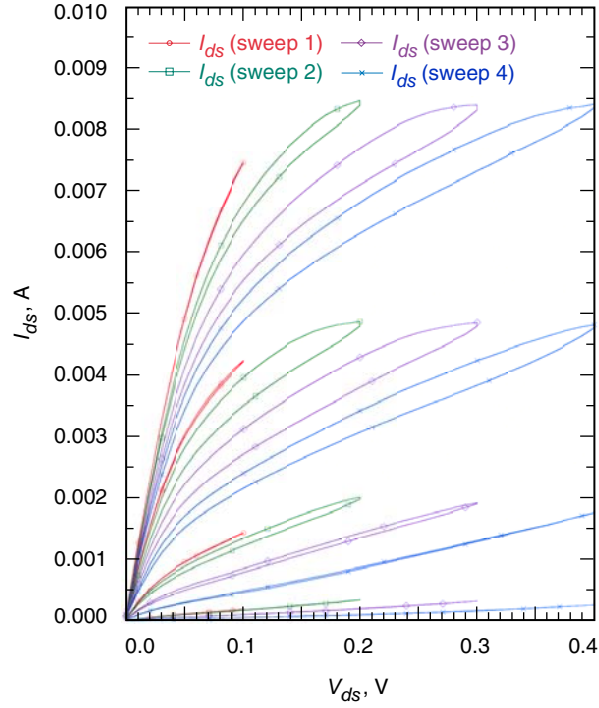


Fig. A-5. Drain current versus drain voltage (double sweeps) for device A, wafer -090, at 15 K, with no light. Four sets of data are shown. In each set of data, the gate voltage ranged from 0.0 to 0.15 V in steps of 0.050 V. Maximum drain voltages were 0.1 V (circle), 0.2 V (square), 0.3 V (diamond), and 0.4 V (X).

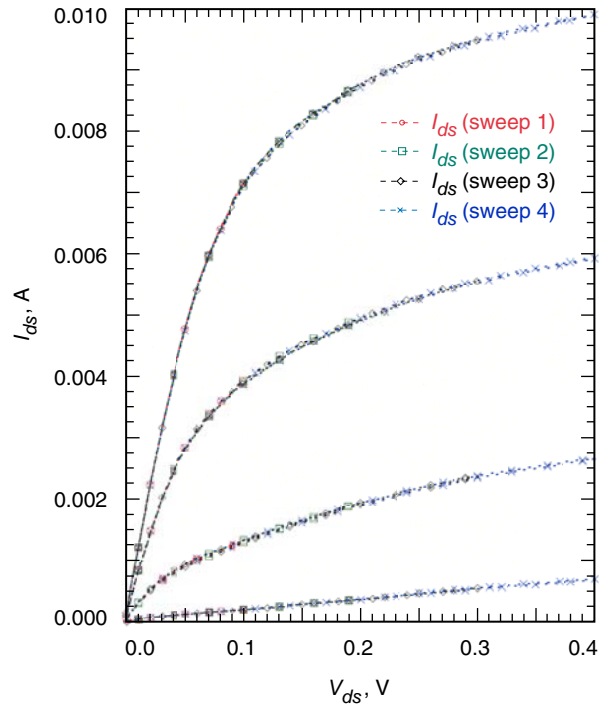


Fig. A-6. The same conditions as shown in Fig. A-5, but with illumination.

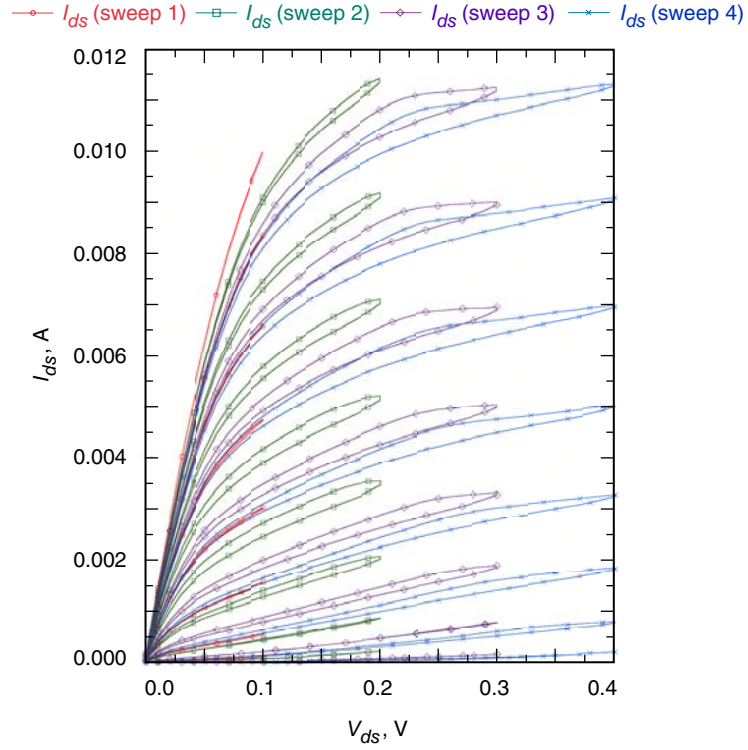


Fig. A-7. Drain current versus drain voltage (double sweeps) for device B, wafer -040, at 15 K, with no light. Four sets of data are shown. In each set of data, the gate voltage ranged from 0.080 to 0.255 V in steps of 0.025 V. Maximum drain voltages were 0.1 V (circle), 0.2 V (square), 0.3 V (diamond), and 0.4 V (X).

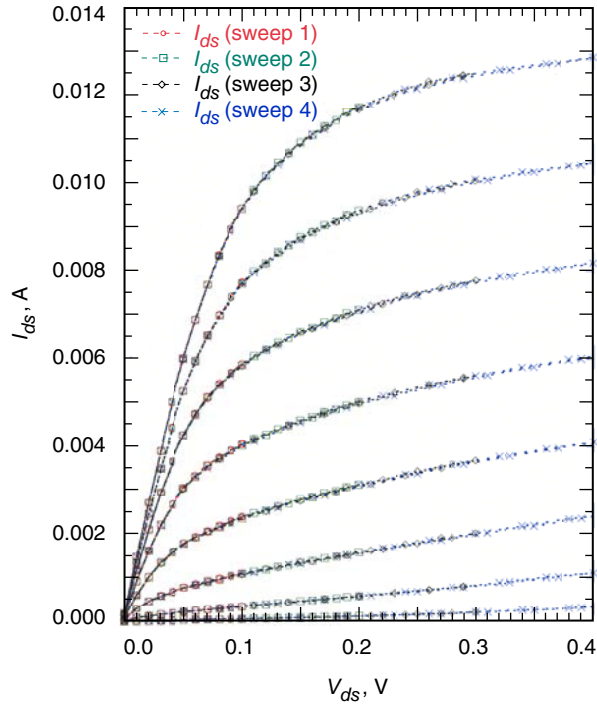


Fig. A-8. The same conditions as shown in Fig. A-7, but with illumination.

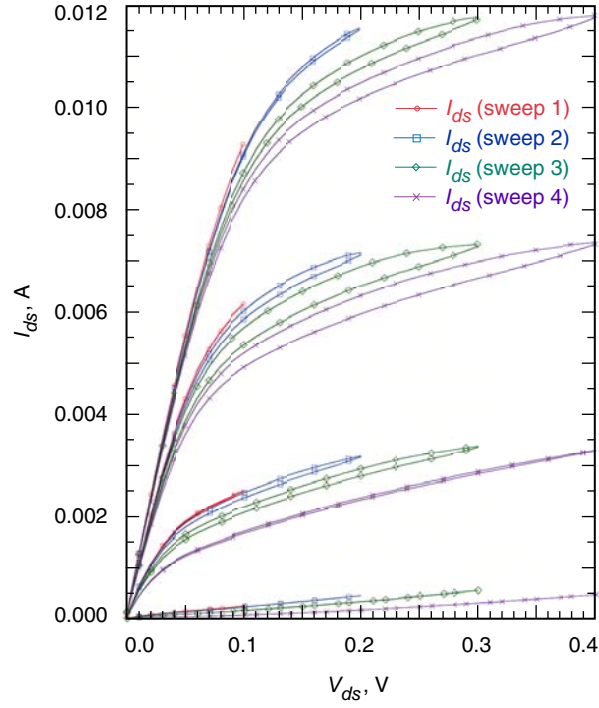


Fig. A-9. Drain current versus drain voltage (double sweeps) for device B, wafer -057, at 15 K, with no light. Four sets of data are shown. In each set of data, the gate voltage ranged from 0.25 to 0.40 V in steps of 0.050 V. Maximum drain voltages were 0.1 V (circle), 0.2 V (square), 0.3 V (diamond), and 0.4 V (X).

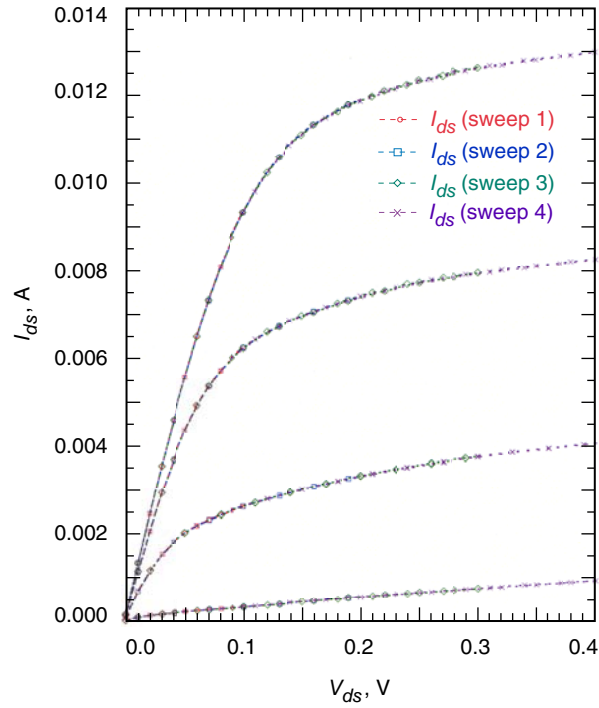


Fig. A-10. The same conditions as shown in Fig. A-9, but with illumination.

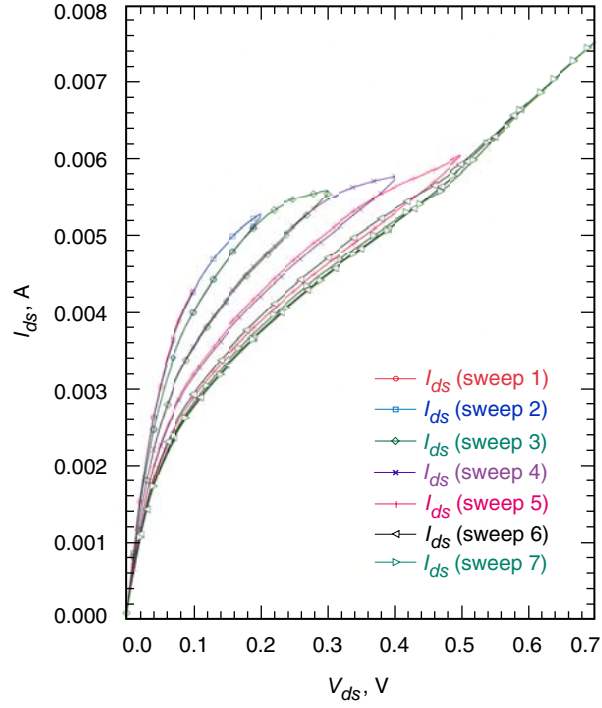


Fig. A-11. Drain current versus drain voltage (double sweeps) for device C, wafer -055, at 15 K, with no light. For sweeps 1 through 7, the maximum drain voltages were 0.1 V (circle), 0.2 V (square), 0.3 V (diamond), 0.4 V (X), 0.5 V (+), 0.6 V (left-pointing triangle), and 0.7 V (right-pointing triangle), respectively. For each sweep, the gate voltage was 0.20 V.